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Dynamic characteristics of neutral beam etching enabled normally-off recessed-gate GaN MOSHEMT

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ABSTRACT

Dynamic performances of recessed-gate GaN metal oxide semiconductor high electron mobility transistors (MOSHEMTs) enabled by argon-based neutral beam etching (Ar-NBE) are comprehensively investigated. Upon positive gate stressing, a minimal shift of + 0.27 V in the threshold voltage (V_{th}) is observed, due to capture of electrons by interface traps at the Al_2O_3/AlGaN interface. Dynamic ON-resistance (R_{on}) and drain current degradation are also studied by applying various drain voltage values and durations. Moreover, interface characterizations by conductance method and deep-level transient spectroscopy (DLTS) both confirm the superior interface quality achieved by NBE processing, with a low interface trap density (D_{it}) of 1.19×10^{12} cm^{-2} eV^{-1}. The results underscore NBE recessing as an attractive approach for manufacturing highly-reliable normally-off GaN MOSHEMTs for next-generation high-frequency power conversion systems.

1. Introduction

Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) are regarded as promising candidates for high-frequency, high-power applications, attributable to wide bandgap, high electron mobility, high critical breakdown electric field (Kozak et al., 2023; Meneghini et al., 2021; Repaka et al., 2024, 2025). In power conversion applications, normally-off devices are highly desirable for fail-safe operations. To achieve this goal, p-GaN gate (Jin et al., 2023; Yang et al., 2024) and recessed-gate have been employed to realize enhancement-mode (E-mode) devices. Compared with p-GaN gate HEMT, recessed-gate metal oxide semiconductor (MOS) HEMTs have gained considerable research interest due to large gate swing and low leakage current (He et al., 2018; Hu et al., 2019; Shi et al., 2016) and impose fewer requirements on starting epi-structure (Hua et al., 2016). Moreover, recessed-gate MOSHEMTs exhibit their multifaceted potential in applications including gas sensor (Raman et al., 2022), power switching (Danielraj et al., 2022), and photodetection (Liu et al., 2024). Cl-based inductively coupled plasma-reactive ion etching (ICP-RIE) has been extensively utilized for the fabrication of recessed-gate structures (Anderson et al., 2016; Liu et al., 2017), however, it may induce plasma-induced damage and dynamic instability (Lin et al., 2017).

Ion beam etching (IBE) or its modified version, argon-based neutral beam etching (Ar-NBE), which features precise material removal via a focused neutral beam of inert gas particles, exhibits substantial promise in providing intricate control over device structures, and alleviating plasma-associated damage (Adesida et al., 1994; Chulukhadze et al., 2023; James et al., 2019; Kuritzky et al., 2016; Ping et al., 1995; Pinto et al., 2022; Pinto Rocha et al., 2023; Smirnov et al., 2016). In recent research, Yu et al. fabricated the recessed-gate MOSHEMT using ICP-RIE and NBE, respectively. The results showed that devices fabricated using the NBE process exhibited an increased current on/off ratio from 10^7 to 10^9 and improved subthreshold swing (S.S.) from 148 mV/dec to 99.6 mV/dec (Yu et al., 2024). Hemmi et al. used pulsed I-V testing to illustrate the influence of NBE process on current collapse of recessed-gate AlGaN/GaN HEMTs. The suppressed current collapse confirmed that NBE has a clear advantage over the conventional ICP etching via mitigating plasma-induced damages (Hemmi et al., 2017). In our previous work, Ar-based NBE was employed in the fabrication of recessed-gate MOSHEMTs, achieving a high threshold voltage (4.22 V), a large current on/off ratio above 10^9, and a low on-state I_G (< 0.6 nA/mm) (Gao et al., 2024) .

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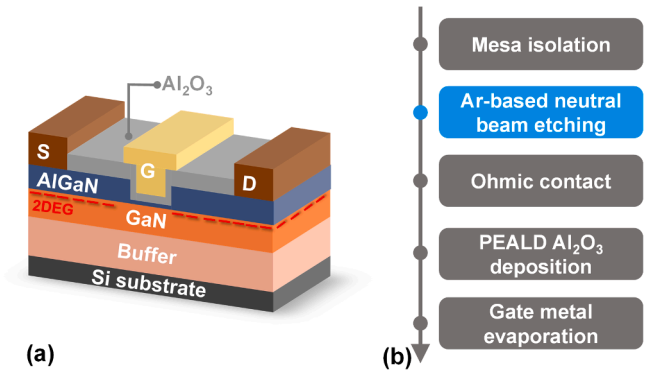

Fig. 1. (a) Schematic structures and (b) fabrication scheme of the recessed-gate GaN MOSHEMT.

Despite the fact that the DC and RF performances of recessed-gate GaN MOSHEMTs by NBE have been reported in our group (Gao et al., 2024; Ye et al., 2025), detailed dynamic characteristics, including time-dependent threshold voltage shift and drain current degradation, have not been thoroughly investigated. Moreover, The interface quality exerts a critical influence on the degradation of MOSHEMT dynamic performance (Lu et al., 2017; Meneghesso et al., 2016; Yao et al., 2022, 2024), thereby necessitating precise interface trap density (D_{it}) quantification as an essential parameter for evaluating interface state.

In this study, normally-off GaN MOSHEMT devices have been successfully fabricated based on an NBE-enabled gate recess step. Additionally, dynamic performance of the recessed-gate MOSHEMTs is thoroughly investigated with different stress conditions. Initially, the time-dependent threshold voltage instabilities upon negative and positive gate stress conditions are investigated. Subsequently, current collapse ratio and dynamic on-resistance (R_{on}) deterioration with off-state drain stress are analyzed using pulse I-V measurements. Moreover, time-dependent device dynamic characteristics, including normalized saturation current/dynamic R_{on} degradation and threshold voltages (V_{th}) shift are investigated. Finally, the D_{it} of the post-etch Al_2O_3/AlGaN interface is characterized using the conductance method and the deep-level transient spectroscopy (DLTS) method, respectively. The good dynamic stability and low D_{it} of the device indicate slight damage after NBE, showing a promising approach to realize high performance recessed-gate GaN MOSHEMTs.

2. Fabrication and measurement

Fig. 1(a) showed the schematic cross section of the recessed-gate GaN MOSHEMT structure employed in this study. The device was grown on a 6-inch Si (111) substrate by metal-organic chemical vapor deposition (MOCVD). The epitaxial layer stack comprised AlN/GaN-based buffer layers, a 200 nm undoped GaN channel layer, a 1 nm AlN spacer layer, a 15 nm undoped $Al_{0.25}Ga_{0.75}$ N barrier layer, and a 2 nm GaN cap layer. As shown in Fig. 1(b), device fabrication process commenced with mesa isolation achieved through Cl-based ICP-RIE. After mesa isolation, Ar-based NBE gate recessing was performed by a 200 eV argon beam, with an etching rate of 3 nm/min for the AlGaN layer. The recessed depth of 12 nm was obtained after 210 s etching process and tetramethylammonium hydroxide (TMAH) treatment, which reduced surface roughness and mitigated etching damage. Ohmic contacts were formed by sequential deposition of 20/150/50/80 nm Ti/Al/Ni/Au layers, followed by annealing at 850 °C in N_2 for 40 s. Subsequently, a 15 nm-thick Al_2O_3 dielectric layer was deposited immediately through plasma-enhanced atomic layer deposition (PEALD) at 300 °C, additionally functioning as a passivation layer for the access regions. Finally, 20/200 nm Ni/Au was deposited to form gate metal and contact pads. The gate length (L_g), gate-source distance (L_{gs}), gate-drain distance (L_{gd}), and gate width (W_g) of the devices were 1.5/3/3/20 μm, respectively. Both electrical static & dynamic properties of the devices, including transfer characteristics, output characteristics, threshold

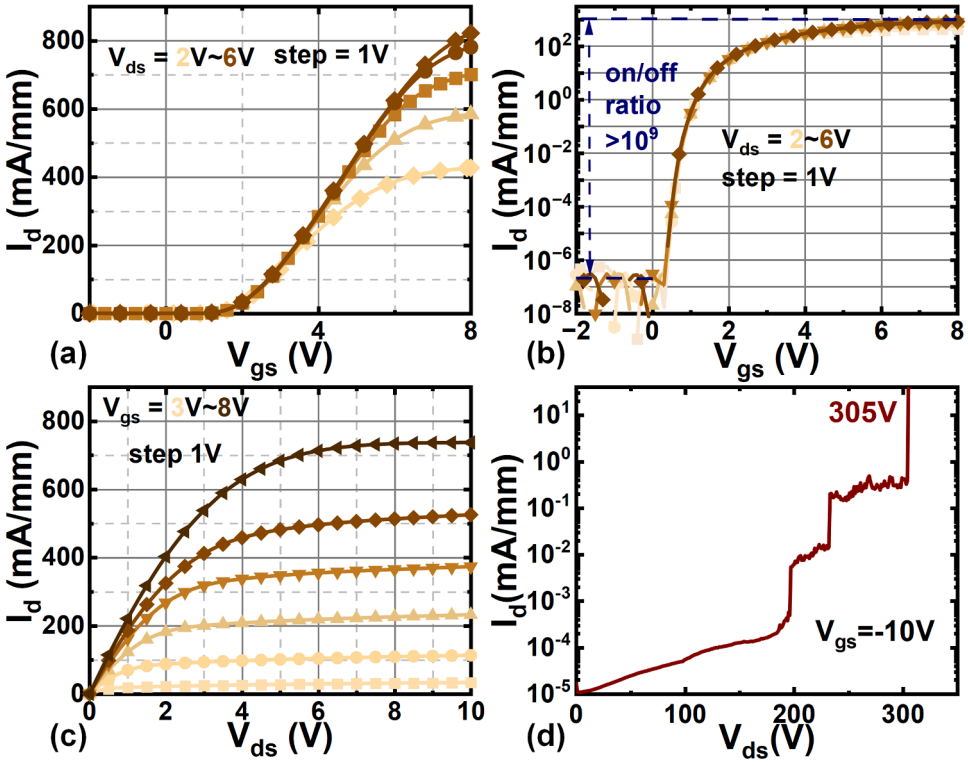

Fig. 2. (a) Linear scale and (b) Log scale Transfer characteristics. (c) Output characteristics, and (d) Off-state breakdown characteristic measured at $V_{gs} = -10$ V for the recessed-gate GaN MOSHEMT.

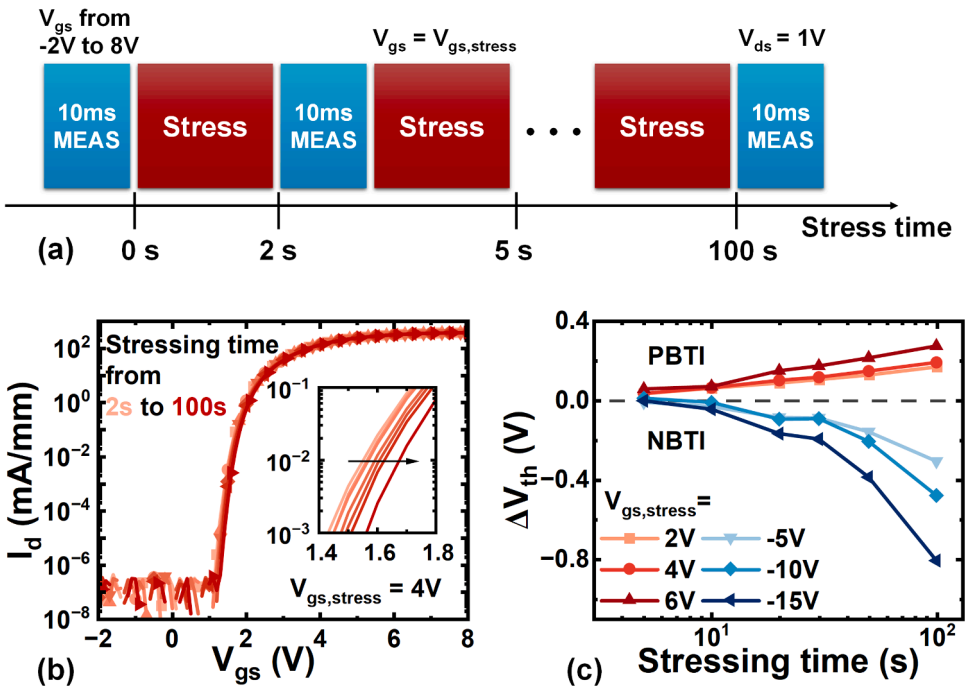

Fig. 3. (a) Schematic describing the M-S-M technique and the associated parameters monitored during the stressing period (b) Transfer characteristics measured during 100 s positive gate bias stressing period ($V_{gs,stress}$ -= 4 V). (c) Variation of V_{th} as a function of stressing time with different gate bias voltage.

voltage instability, pulsed I-V characteristics, and time-resolved drain current (I_d) & R_{on} were explicitly characterized.

3. Result and discussion

3.1. Static DC characteristics

Fig. 2(a) illustrated the linear scale transfer characteristics of recessed-gate GaN MOSHEMT at room temperature. The V_{th} of device was extracted to be 1.82 V at V_{ds} = 2 V, defined at I_d of 1 mA/mm from the transfer curves. As shown in Fig. 2(b), the on/off drain current ratio could be extracted as 4.8 × 10^9 from log scale transfer characteristics. The output characteristics of device were presented in Fig. 2(c), the device exhibited an R_{on} of 4.54 Ω•mm and a high saturation I_d density of 737 mA/mm at V_{gs} = 8 V. Fig. 2(d) showed the off-state breakdown characteristic of device showing off-state breakdown voltage of 305 V.

3.2. Dynamic performance

Positive and negative bias-induced threshold instability (PBTI and NBTI) were investigated utilizing the measure-stress-measure (M-S-M) technique (Meneghini et al., 2016), which involves periodically interrupting the stressing phases to perform rapid I_D-V_G measurements. Fig. 3(a) showed the schematic describing the M-S-M process, rapid measurement duration of 10 ms ensures that the trap behavior upon the stressing stage is not affected. During each fast measurement period, V_{gs} was swept from −2 V to 8 V while maintaining V_{ds} to be 1 V. Various gate stressing voltages were set during stressing period while drain was grounded. The total stressing time was set as 100 s to ensure that the effect of traps on device degradation was vastly taken into account. Fig. 3(b) illustrated the multiple transfer characteristics measured during 100 s positive gate bias stressing period with gate stress voltage ($V_{gs,stress}$) of 4 V. The V_{th} showed a slight positive shift during positive gate bias stressing period. A small V_{th} shift of 0.18 V could be obtained when $V_{gs,stress}$ = 4 V and stressing time = 100 s. Moreover, the stress conditions were varied to further investigate the V_{th} shift characteristics. With positive stress conditions, the $V_{gs,stress}$ was changed from 2 V to 5 V, while upon negative stress conditions, the $V_{gs,stress}$ ranged from −5 V to −15 V. The relationship between the V_{th} shift and stress time is illustrated in Fig. 3(c). When a positive gate stress was applied, the V_{th} exhibited a positive shift. Specifically, with $V_{gs,stress}$ of 2 V, the V_{th} shifted positively by 0.17 V; when the $V_{gs,stress}$ increased to 6 V, the V_{th} shift rose to 0.27 V. Conversely, with negative gate stress, the V_{th} showed a negative shift. For $V_{gs,stress}$ of −5 V applied for 100 s, the V_{th}

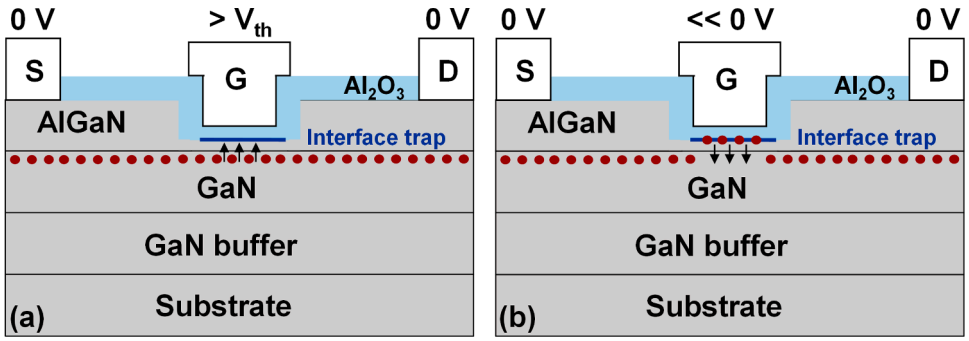

Fig. 4. Schematic illustration of trapping mechanisms with (a) positive gate stressing condition and (b) negative gate stressing condition.

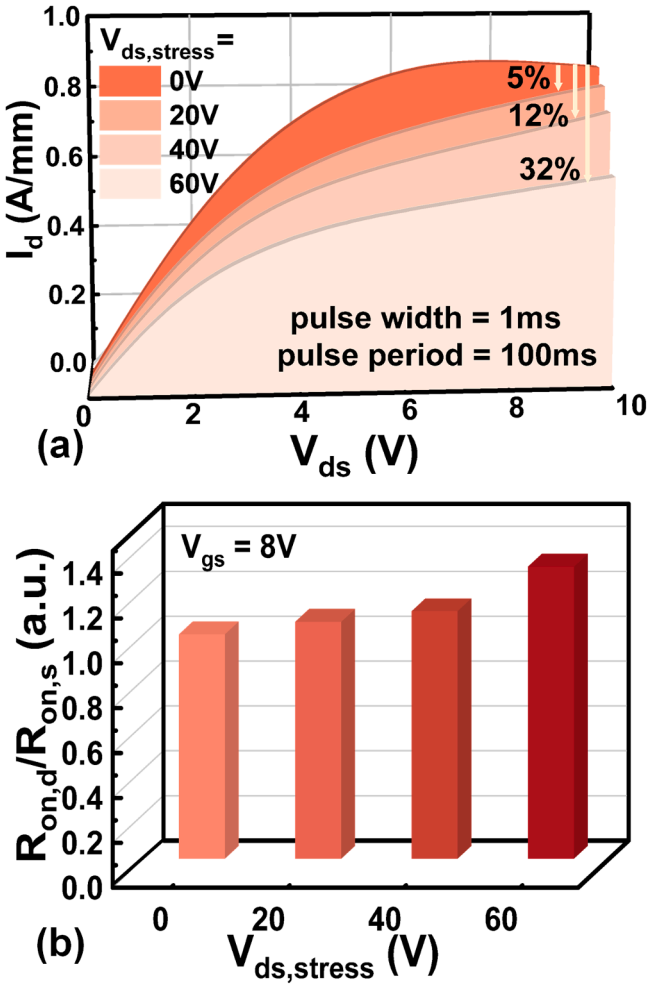

Fig. 5. (a) Pulse output characteristics with different off state drain stress voltage, gate bias voltage is fixed at 0 V, drain stress voltage ($V_{ds,stress}$) is increased from 20 V to 60 V. (b) Ratio of dynamic R_{on}/static R_{on} with different off state drain stress voltage.

shifted by −0.3 V. Even with the stress voltage increased to −15 V, the V_{th} shifted by only −0.80 V after 100 s of stress. Fig. 4 showed the schematic illustration of trapping mechanisms with gate stressing condition. The V_{th} shift induced by gate stress is associated with the trapping/detrapping at the interface between the dielectric layer and the barrier layer in devices (Hori et al., 2013; Lu et al., 2013; Yang et al., 2017; Zhang et al., 2023; Zhu et al., 2018). When a positive $V_{gs,stress}$ was applied, electrons in the 2DEG channel are trapped in the interface traps, reducing the number of free electrons in the channel. The trapped electrons also exerted a repulsive force on the remaining free electrons in the channel, resulting in a positive shift in V_{th}, thus requiring a higher voltage to turn the device on. On the contrary, with negative $V_{gs,stress}$, the electrons previously trapped at the interface were released, reducing or eliminating their repulsive effect on the channel electrons, which leads to a negative shift in V_{th}, making the device easier to turn on. The trapping and detrapping processed at the interface are influenced by the magnitude of the stress voltage, with higher voltages accelerating these processes.

Fig. 5(a) showed the pulsed output characteristics of device with various off-state drain stress voltage ($V_{ds,stress}$). During stress phase, drain was applied with a large $V_{ds,stress}$ while source and gate were grounded to common voltage to ensure that device in the off-state. The measurement drain voltage changed from 0 V to 10 V, moreover, measurement gate voltage was set to 8 V. Due to the limitation of the instrument, the pulse period and pulse width were set to 100 ms and 1 ms,

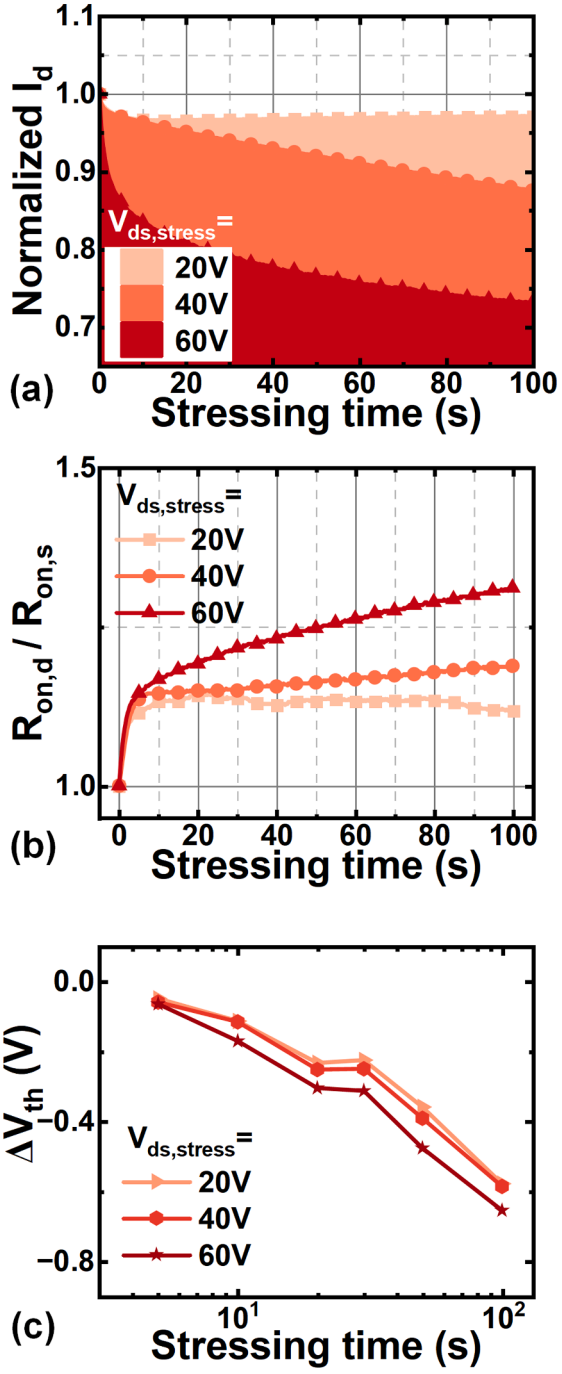

Fig. 6. Variation of (a) normalized I_d, (b) ratio of $R_{on,d}/R_{on,s}$ and (c) V_{th} instability as a function of stressing time at different off state drain stress voltage.

respectively. The current collapse ratio become worse as $V_{ds,stress}$ increased from 20 V to 60 V. When $V_{ds,stress}$ = 20 V, a small current collapse of 5.2 % could be observed. As $V_{ds,stress}$ increased to 60 V, the current collapse worsened to 32.3 %. In addition, The results of dynamic R_{on} ratio degradation with different $V_{ds,stress}$ conditions were illustrated in Fig. 5(b). The dynamic R_{on} ratio was defined as ($R_{on,d}/R_{on,s}$), where $R_{on,s}$ was extracted in the fresh state [($V_{gs,stress}$, $V_{ds,stress}$) = (0 V, 0 V)] and $R_{on,d}$ was extracted in the stressing condition. R_{on} was measured in the linear region of output curve, and the measurement voltage of the device was V_{gs} = 8 V and V_{ds} = 1 V. For this device, the dynamic R_{on} ratio increased from 1.05 to 1.30 as $V_{ds,stress}$ changed from 20 V to 60 V.

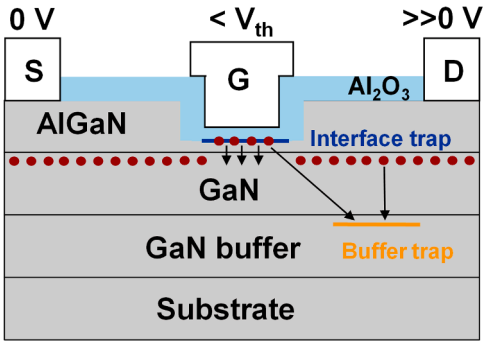

Fig. 7. Schematic illustration of trapping mechanisms with off-state drain stressing condition.

Fig. 6 showed the time-dependent instabilities of device with the same off-state drain stress condition as pulse I-V test. The normalized saturation current trainset in 100 s stress period with different $V_{ds,stress}$ was illustrated in Fig 6(a). In measurement period, I_d was measured in the saturation region of output curves ($V_{gs,m}$ = 8 V, $V_{ds,m}$ = 10 V). Normalized I_d was defined as ($I_{d,dynamic}/I_{d,static}$), where $I_{d,static}$ was measured in the fresh state. With the off-state drain stress, the device normalized I_d decreased gradually. Notably, with $V_{ds,stress}$ of 20 V for a duration of 100 s, the normalized I_d exhibited a reduction of merely 3 %. Upon increasing the $V_{ds,stress}$ to 40 V, a modest alteration in the saturation current, quantified at 12 % was observed. Even with the $V_{ds,stress}$ increased to 60 V, the degradation of the normalized I_d remains limited, showing a reduction of only 27 %. Fig. 6(b) showed dynamic R_{on} ratio as a function of stressing duration, where R_{on} was extracted in the linear region of output curve ($V_{gs,m}$ = 8 V, $V_{ds,m}$ = 1 V). The dynamic R_{on} ratio progressively deteriorates over time with the off-state $V_{ds,stress}$. In case of $V_{ds,stress}$ = 20 V, the dynamic R_{on} ratio exhibited minimal change, maintaining a value as low as 1.09 after a stressing duration of 100 s. As $V_{ds,stress}$ increased to 40 V and 60 V, the dynamic R_{on} ratio was observed to be 1.19 and 1.31, respectively. The degradation of the saturation current and dynamic R_{on} ratio induced by off-state $V_{ds,stress}$ was associated with traps in the access region. Fig. 7 showed the schematic illustration of trapping mechanisms with off-state drain stressing condition. Under the influence of a lateral electric field, electrons were captured by these traps. These electrons originated from the release of electrons from interface traps and 2DEG. The captured electrons contributed to an increase in the resistance of the conduction channel, leading to a reduction in current.

Fig. 6(c) illustrated the V_{th} shift as a function of stressing time with off-state $V_{ds,stress}$. Upon application of $V_{ds,stress}$, the V_{th} demonstrated a gradual negative shift. Specifically, the V_{th} had a −0.6 V shift after 100 s stressing time with $V_{ds,stress}$ of 20 V. As $V_{ds,stress}$ increased to 60 V, the V_{th} shift remains limited to a leftward movement of only 0.65 V. The V_{th} shift induced by off-state $V_{ds,stress}$ was attributed to the interface traps located between the dielectric layer and the barrier layer under the gate region. As shown in Fig. 7, when off-state $V_{ds,stress}$ was applied, the resultant gate-channel vertical electric field facilitated the release of captured electrons from the interface traps. The release of these captured electrons consequently resulted in a negative shift of the V_{th}. This phenomenon was analogous to the effects observed with negative $V_{gs,stress}$, as both stress conditions generate gate-channel vertical electric field in the same direction. Related research shows that adding a field plate could effectively reduce peak of the localized electric field and mitigates the trapping of charge, which results in an increased V_{th} stability with off-state $V_{ds,stress}$ (Hu et al., 2019; Wu et al., 2021).

3.3. Interface trap analysis

To investigate the distribution of interface states between Al_2O_3 dielectric and AlGaN barrier layer after etching, we used the recessed

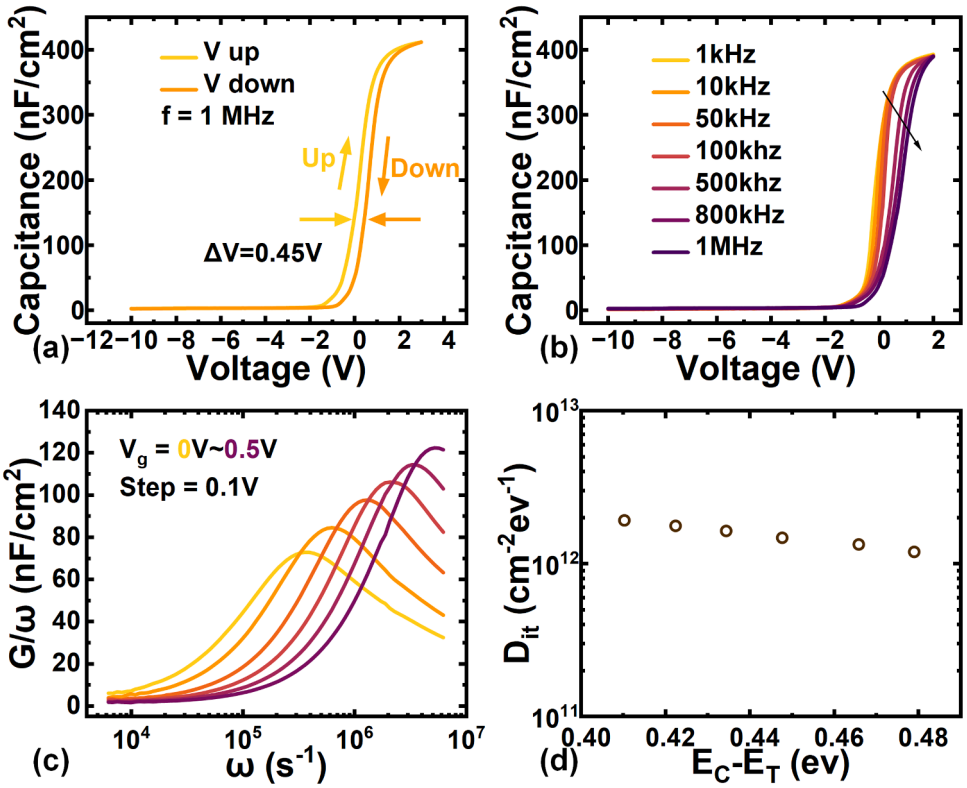

Fig. 8. (a) Double sweep C–V characteristics of gate recessed Al_2O_3 MOSCAP at 1 MHz. (b) C–V characteristics of gate recessed Al_2O_3 MOSCAP from 10 kHz to 1 MHz. (c) Parallel conductance as a function of radial frequency with different bias voltages (d) Gate recessed interface trap state density with trap energy levels below the conduction band edge.

Table 1
Comparison of D_{it} values measured for devices with different recessed-gate etching processes

Ref	Etching process	Dielectric	$D_{it}(cm^{-2}eV^{-1})$
This work	Ar-NBE	15 nm Al_2O_3	1.19×10^{12}
(Yu et al., 2024)	NBE	30 nm HfO_2	1.23×10^{13}
(Huang et al., 2023)	Self-terminating Wet Etching	5 nm AlN+ 30 nm SiN_x	$1.91 \times 10^{12*}$
(Hu et al., 2019)	ALE	15 nm HfSiO	5.9×10^{12}
(He et al., 2021)	SAG	30 nm Al_2O_3	$7.51 \times 10^{12*}$

*Estimated value.

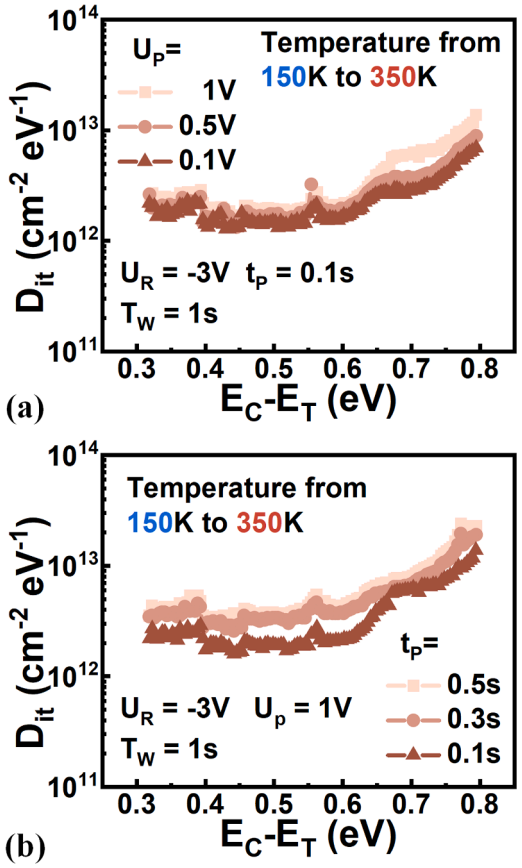

Fig. 9. Interface trap state density of recessed-gate GaN MOSCAPs measured by DLTS with (a) different pulse voltage (U_P) and (a) different pulse width (t_P). U_R is the reverse bias and T_W is the measurement time.

Al_2O_3/AlGaN/GaN metal-oxide-semiconductor capacitor (MOSCAP) with a more symmetrical structure to evaluate the interface states. Double sweep capacitance-voltage hysteresis characteristic at 1 MHz is plotted in Fig. 8(a). A hysteresis of 0.45 V is observed for positive gate bias. Fig. 8(b) and (c) show the multi-*f* C-V and G/ω-ω characteristics of the Al_2O_3/AlGaN/GaN MOSCAP with the measurement frequency ranging from 10 kHz to 1 MHz. There is one rising slope in the multi-*f* C-V characteristics, where the rising slope is near the V_{TH} of recessed-gate MOS-HEMT. Then the conductance method is used to detect the interface states at dielectric/barrier, where the measurement bias voltage is set at the rising slope (Yang et al., 2015). Fig. 8(c) demonstrates the G/ω as a function of ω, and the peak of G/ω moves to a higher frequency. Using the parallel conductance method, interface trap densities are extracted, ranging from 1.91×10^{12} to 1.19×10^{12} cm^{-2} eV^{-1} with trap levels spanning from 0.40 eV to 0.48 eV below the conduction band as shown in Fig. 8(d). Table 1 showed the comparison of D_{it} values measured for devices with different recessed-gate etching processes. A device using NBE , which realized by neutralization of negative ions, had the D_{it} of 1.23×10^{13} cm^{-2} eV^{-1} (Yu et al., 2024). Devices with self-terminating wet etching (Huang et al., 2023) and atomic layer etching (ALE) (Hu et al., 2019) illustrated the D_{it} of 1.91×10^{12} cm^{-2} eV^{-1} and 5.9×10^{12} cm^{-2} eV^{-1}, respectively. Device employing selective-area growth (SAG) to achieve normally-off showed the D_{it} of 7.51×10^{12} cm^{-2} eV^{-1} (He et al., 2021). These results proved that Ar-NBE technology mitigates etch damage and achieves good interface quality.

Furthermore, the wide mapping of the continuum interface traps at Al_2O_3/AlGaN was evaluated by deep-level transient spectroscopy (DLTS) (Lang, 1974; Deng et al., 2023) in Fig. 9. By varying temperature from 200 to 350 K, the D_{it} was extracted from 0.3 to 0.8 eV. The amplitude of D_{it} is proportional to the DLTS signal, as follows Eq. (1):

$$D_{it} = \frac{\varepsilon A N_S C_{ox} b_1}{kTC_M^3 \ln\left(\frac{t_2}{t_1}\right)} \quad (1)$$

where the $\varepsilon=\varepsilon_s\varepsilon_0$, C_{ox} is the capacitance of the oxide layer, C_M is the capacitance at measured voltage V_m, k is the Boltzmann constant, T is temperature, t_2 and t_1 are the chosen measurement and sampling times. It can be observed that more interface states are detected with larger energy level. As shown in Fig. 9(a), when U_P increases from 0.1 V to 1 V, the value of D_{it} at 0.5 eV increases from 1.51×10^{12} $cm^{-2}eV^{-1}$ to 1.95×10^{12} $cm^{-2}eV^{-1}$. The higher D_{it} with higher U_P indicates more injection of carriers induced by the larger forward bias. As shown in Fig. 9(b), when t_P increases from 0.1 s to 0.5 s, the value of D_{it} at 0.5 eV increases from 1.95×10^{12} $cm^{-2}eV^{-1}$ to 3.80×10^{12} $cm^{-2}eV^{-1}$. The higher D_{it} with longer t_P indicates more injection of carriers induced by the longer injection time. When t_P is 0.1 s, 0.3 s and 0.5 s, the value of D_{it} at 0.32 eV is 2.19×10^{12} $cm^{-2}eV^{-1}$, 3.47×10^{12} $cm^{-2}eV^{-1}$ and 3.55×10^{12} $cm^{-2}eV^{-1}$, and the value of D_{it} at 0.79 eV is 1.38×10^{13} $cm^{-2}eV^{-1}$, 1.91×10^{13} $cm^{-2}eV^{-1}$ and 2.29×10^{13} $cm^{-2}eV^{-1}$, respectively. It can be found that the value of D_{it} rises rapidly below 0.3 s and climbs slowly after 0.3 s at 0.32 eV, while it increases uniformly at 0.79 eV. The different phenomenon demonstrates that 0.3 s is long enough to fill most of the interface states with lower energy level and more injection time is necessary to fill most of the interface states with higher energy level. Compared to the conductance method, interface traps with longer time constants and deeper levels can be extracted by DLTS. The relatively low level of interface trap density indicated that ion beam etching results in superior interface quality, which corresponds to the stability of the devices.

4. Conclusion

This study demonstrates solid dynamic reliability of recessed-gate GaN MOSHEMTs fabricated via Ar-NBE. When a positive $V_{gs,stress}$ of 6 V was applied, the threshold voltage exhibited a slight positive shift of 0.27 V over a 100 s stressing period. In addition, a −0.80 V negative shift of V_{th} was observed with a negative $V_{gs,stress}$ of −15 V. The gate bias induced V_{th} shifts were related to the interface trap locating in Al_2O_3/AlGaN interface. Meanwhile, during 100 s stressing period with off-state $V_{ds,stress}$ of 60 V, saturation current decreased by 27 % and dynamic R_{on} ratio was degraded to 1.31, both resulting from electron trapping at the access region. Moreover, the interface trap state density of post-etch Al_2O_3/AlGaN interface was investigated utilizing conductance method and DLTS analyses. The results indicate that the interface state density is comparatively low, at the order of 10^{12} cm^{-2} eV^{-1}, which matches well the steady dynamic characteristics of the device. These results elucidate that the technique of Ar-based NBE gate recessing presents a viable and promising method for fabricating high-performance normally-off GaN MOSHEMTs, which are highly demanded power conversion applications as well as in all-GaN monolithic integration.

CRediT authorship contribution statement

Yitai Zhu: Writing – review & editing, Writing – original draft, Visualization, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Haitao Du:** Writing – review & editing, Methodology, Conceptualization. **Yu Zhang:** Writing – review & editing, Writing – original draft, Methodology, Data curation, Conceptualization. **Haolan Qu:** Writing – review & editing, Methodology. **Han Gao:** Writing – review & editing, Conceptualization. **Haodong Jiang:** Writing – review & editing, Methodology. **Wenhui Xu:** Resources, Methodology. **Xin Ou:** Resources, Methodology. **Xinbo Zou:** Writing – review & editing, Supervision, Resources, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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